

alternative embodiment illustrated in FIG. 3, the field plate 15 is connected to a gate bond contact area 13 a certain distance from the edge termination. The field plate 15 is also connected to the gate electrodes 10 in the cell field. This figure illustrates the usual position 15 of a gate bond contact area. In this position traditional conductive areas in the edge termination are covered with insulators to prevent electrical arc-over and leakage currents, and are not therefore accessible for connection to a bonding wire. The n⁺-doped zone 21 indicated in FIG. 3 is optional and further promotes an increase in the reverse transfer capacitance C_{GD} of the semiconductor device.

[0035] FIG. 4 illustrates a schematic cross-section through a semiconductor device 3 as disclosed in a further embodiment. Components with functions identical to those illustrated in the preceding figures are indicated by using the same reference numerals and are not described in greater detail here. The structure of the semiconductor device 3 illustrated in FIG. 4 corresponds to that previously illustrated in FIG. 1, although in order to achieve a smooth transition region of the equipotential lines 25 and 31 from the cell field 9 to the edge region 12 the charge compensation zones 22 are configured such that they are positioned at almost constant stepwidth P as in the central cell field 9, and the width b is kept as in the cell field, but the depth t_z of the charge compensation zones with body zone in the cell region 9 is reduced from t_1 via t_2 to t_3 . This has a similar effect on the equipotential lines as the reduction of the width b of the charge compensation zones 22 at constant depth t .

[0036] FIG. 5 illustrates a schematic cross-section through a semiconductor device 4 as disclosed in a further embodiment. In this semiconductor device 4 a voltage-receiving zone 23 in the transition region 30 between the cell field 9 and the edge region 12 is provided with increased oxide thickness at the transition 30 from the cell field 9 to the edge region 12 by giving the field plate 15 a recess 24. This prevents a sharp curve in the equipotential surface 31, as illustrated in FIG. 2 at the transition from the n⁺-conducting edge zone to the n⁺-conducting highly doped zone 21, thereby reducing voltage spikes. In this arrangement, the field plate regions are electrically connected to the gate bond contact area 13 before and after the recess 24. Thanks to this voltage-reducing region 23 it is possible to achieve a relatively thin field plate oxide 18, the n⁺-conducting, highly doped zone 21 in the edge region simultaneously ensuring that the equipotential line 25 is shifted out of the semiconductor body 6 to the field plate oxide 18 near the surface.

[0037] Thus the high field strengths occurring inside the semiconductor to the right and left of the n⁺-conducting zone 21 forming the drain-side electrode of the capacitor are reduced. As a result the blockability of the semiconductor device 4, which might otherwise be reduced at these points by the voltage-receiving region 23 consisting of the semiconductor over a transition region 30 which also has a thick intermediate insulating layer, is completely removed from the low doped semiconductor region. Only outside this transition region does the voltage then fall due to a thin dielectric layer made of field plate oxide 18. The left-hand region of the field plate structure 15 bonded by the contact via 16 in FIG. 5 is illustrated with a relatively small surface area. In one embodiment, it may cover a large area of the edge region 12.

[0038] In this arrangement, the n⁺-conducting zone 21 stops the electrical field from penetrating the semiconductor body 6 in this zone 21, thereby preventing any collision

ionisation which might reduce blockability. This embodiment as illustrated in FIG. 5 achieves an improved transition 30 from the cell field 9 to a highly doped n⁺-conducting zone 21 near the surface of the semiconductor body 6. The masks for the field plate structure 15 in the edge region 12 of the semiconductor device 4 must therefore be adapted accordingly.

[0039] Instead of the variation in the widths of the charge compensation zones illustrated in FIG. 5 which ensure smoother radii of curvature of the equipotential lines in the transition region 30, it is also possible to combine charge compensation zones with variable penetration depth as illustrated in FIG. 4, and with a voltage-receiving region 23.

[0040] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A semiconductor device with a charge carrier compensation structure comprising:
 - a central cell field with a gate structure and a source structure;
 - an edge region associated with the cell field;
 - bond contact areas in the edge region electrically coupled to the gate structure or to the source structure; and
 - a capacitance increasing field plate electrically coupled to at least one of the bond contact areas.
2. The semiconductor device of claim 1, wherein the capacitance increasing field plate is positioned beneath the gate bond contact area and set to gate potential by contact vias through an intermediate oxide.
3. The semiconductor device of claim 1, wherein the capacitance increasing field plate is positioned beneath the source bond contact area and set to source potential by contact vias through an intermediate oxide.
4. The semiconductor device of claim 1, wherein the capacitance increasing field plate is electrically coupled to near-edge planar or trench gate electrodes of the cell field and to the gate bond contact area.
5. A semiconductor device with a charge carrier compensation structure in a semiconductor body comprising:
 - a central cell field with a near-surface gate- and source structure;
 - an edge region lying adjacent to and/or in the cell field;
 - bond contact areas in the edge region which are electrically connected to the gate structure or to the source structure; and
 - there being positioned under at least one part of at least one of the bond contact areas a laterally extending, capacitance-increasing field plate which is insulated from the semiconductor body and electrically connected to at least one of the near-surface bond contact areas.
6. The semiconductor device of claim 5, wherein there is positioned between the upper side of the semiconductor body and the capacitance-increasing field plate a field plate oxide of a thickness greater than the thickness of a gate oxide.
7. The semiconductor device of claim 5, wherein sharp radii of curvature of the equipotential lines/equipotential sur-